AMENDMENTS TO THE CLAIMS

1. (Currently amended) An input circuit that is arranged for rail-to-rail operation with a differential input signal, comprising:

a differential input circuit for receiving the differential input signal, wherein the differential input circuit ~~signal~~ is configured to provide:

a first positive differential current in response to the differential input signal, and

a first negative differential current in response to the differential input signal;

a differential trim circuit for enabling trimming of an offset, wherein the differential trim circuit is configured to provide:

a second positive differential current in response to a differential positive trim signal; and

a second negative differential current in response to a differential negative trim signal; and

a current mirror stage for enabling a transconductance of the input circuit to be relatively constant for a common mode voltage of the differential input signal, comprising:

a first current mirror circuit that is configured to receive a first current that is related to the common mode voltage, wherein the first current mirror circuit is further configured to reflect the first current to provide a first positive tail current to the differential input circuit, and further configured to reflect the first current to provide a second positive tail current to the differential trim circuit; and

a second current mirror circuit that is configured to receive a second current that is related to the common mode voltage, wherein the second current mirror circuit is further configured to reflect the second current to provide a first negative tail current to the differential input circuit, and further configured to reflect the first current to provide a second negative tail current to the differential trim circuit; and

an output stage for providing differential output currents.

2. (Original) The input circuit of Claim 1, further comprising:

a comparison differential pair that is configured to receive a reference signal at a first gate of the comparison differential pair and further configured to receive a compared signal at a second gate of the comparison differential pair, wherein the compared signal is related to the common mode voltage of the differential input signal, and wherein the comparison differential pair is configured to provide the second current and a third current.

3. (Original) The input circuit of Claim 2, further comprising:

a third current mirror circuit that is configured to reflect the third current to provide the first current.

4. (Original) The input circuit of Claim 1, wherein the differential trim circuit is a replica of the differential input circuit, scaled by a factor.

5. (Original) A CMOS input circuit that is arranged for rail-to-rail operation with a differential input signal, comprising:

a differential input circuit for receiving the differential input signal, comprising:

a PMOS differential input stage that is arranged to provide a first PMOS differential current in response to the differential input signal; and

an NMOS differential input stage that is arranged to provide a first NMOS differential current in response to the differential input signal;

a differential trim circuit for enabling trimming of an offset, comprising:

a PMOS differential trim stage that is arranged to provide a second PMOS differential current in response to a differential PMOS trim signal; and

an NMOS differential trim stage that is arranged to provide a second NMOS differential current in response to a differential NMOS trim signal; and

a current mirror stage for enabling a transconductance of the input circuit to be relatively constant for a common mode voltage of the differential input signal, comprising:

a first current mirror circuit that is configured to receive a first current that is related to the common mode voltage, wherein the first current mirror circuit is further configured to reflect

the first current to provide a first PMOS tail current to the PMOS differential input stage, and further configured to reflect the first current to provide a second PMOS tail current to the PMOS differential trim stage; and

a second current mirror circuit that is configured to receive a second current that is related to the common mode voltage, wherein the second current mirror circuit is further configured to reflect the second current to provide a first NMOS tail current to the NMOS differential input stage, and further configured to reflect the first current to provide a second NMOS tail current to the NMOS differential trim stage; and

an output stage for enabling the first PMOS differential current and the second PMOS differential current to be combined to provide a PMOS differential output current, and further enabling the first NMOS differential current and the second NMOS differential current to be combined to provide a NMOS differential output current.

6. (Original) The input circuit of Claim 5, further comprising:

a comparison differential pair that is configured to receive a reference signal at a first gate of the comparison differential pair and further configured to receive a compared signal at a second gate of the comparison differential pair, wherein the compared signal is related to the common mode voltage of the differential input signal, and wherein the comparison differential pair is configured to provide the second current and a third current.

7. (Original) The input circuit of Claim 6, further comprising:

a third current mirror circuit that is configured to reflect the third current to provide the first current.

8. (Original) The input circuit of Claim 5 further comprising a summer circuit, wherein the summer circuit is further configured to provide a differential output current in response to the output PMOS differential current and the output NMOS differential current such that the differential output current is approximately equal to the sum of the output PMOS differential current and the output NMOS differential current.

9. (Original) The input stage of Claim 8, wherein the summer circuit comprises a folded cascode amplifier circuit.

10. (Original) The input circuit of Claim 5, wherein the PMOS differential input stage comprises a PMOS differential pair.

11. (Original) The input circuit of Claim 10, wherein:
the NMOS differential input stage comprises an NMOS differential pair.

12. (Original) The input circuit of Claim 5, wherein:
the output stage comprises a first node, a second node, a third node, and a fourth node;
the PMOS differential input stage is configured provide the first PMOS differential current at the first and second nodes;
the first NMOS differential input stage is configured to provide the first NMOS differential current at the third node and fourth nodes;
the PMOS differential trim stage is arranged to provide the second PMOS differential current at the first and second nodes; and
the NMOS differential trim stage is arranged to provide the second NMOS differential current at the third and fourth nodes.

13. (Original) The input circuit of Claim 5, wherein the differential trim circuit is a replica of the differential input circuit, scaled by a factor.

14. (Original) The input circuit of Claim 13, wherein the first current mirror circuit is configured to provide the first PMOS tail current and the second PMOS tail current such that the ratio of the second PMOS tail current to the first PMOS tail current corresponds to the factor, and wherein the second current mirror circuit is configured to provide the first NMOS tail current and

the second NMOS tail current such that the ratio of the second NMOS tail current to the first NMOS tail current corresponds to the factor

15. (Original) The input circuit of Claim 5, wherein the differential input circuit and the differential trim circuit each comprises transistors that are biased for subthreshold operation.

16. (Currently amended) A method employing an input circuit to provide ~~for providing~~ a differential output current in response to a differential input signal, the method comprising:

receiving the differential input signal via a rail-to-rail CMOS input stage;

trimming an offset of the differential input signal such that accuracy over temperature is approximately maintained; and

enabling a ~~the~~ transconductance of the input circuit to be relatively constant for a common mode voltage of the differential input signal.

17. (Original) The method of Claim 16, further comprising:

providing a first PMOS differential current in response to the differential input signal; and

providing a first NMOS differential current in response to the differential input signal;

wherein trimming is accomplished via a differential trim circuit that is a scaled replica of the CMOS input stage, and wherein trimming comprises:

providing a second PMOS differential current in response to a differential PMOS trim signal

providing a second NMOS differential current in response to a differential NMOS trim signal;

summing the first PMOS differential current to the second PMOS differential current to provide a PMOS differential output current; and

summing the first NMOS differential current to the second NMOS differential current to provide an NMOS differential output current.

18. (Original) The method of Claim 17, further comprising:

summing the PMOS differential output current and the NMOS differential output current to provide the differential output current.

19. (Original) The method of Claim 16, wherein enabling comprises:

comparing a compared signal that is related to a common mode voltage of the differential input signal to a reference signal;

providing a first current and a second current in response to the comparison;

reflecting the first current to provide a third current;

reflecting the third current to provide a first PMOS tail current;

reflecting the third current to provide a second PMOS tail current such that the ratio of the first PMOS tail current and the second PMOS tail current corresponds to a factor;

reflecting the second current to provide a first NMOS tail current;

reflecting the second current to provide a second NMOS tail current such that the ratio of the first NMOS tail current and the second NMOS tail current corresponds to the factor;

driving the CMOS input stage with the first NMOS tail current and the second NMOS tail current; and

driving a differential trim circuit with the first PMOS tail current and the second NMOS tail current, wherein the second PMOS and NMOS differential currents are provided via the differential trim circuit, and wherein the differential trim circuit is a replica of the CMOS input stage that is scaled by the factor.

20. (Currently amended) An input circuit for rail-to-rail operation with a differential input signal, comprising:

a means for trimming an offset of the differential input signal such that accuracy over temperature is approximately maintained; and

a means for enabling a ~~the~~ transconductance of the input circuit to be relatively constant for a common mode voltage of the differential input signal.

21. (New) The input circuit of Claim 20, further comprising:

means for biasing the input circuit in subthreshold.

22. (New) The method of Claim 16, further comprising:

biasing the rail-to-rail CMOS input stage in subthreshold.